AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A device for controlling a frequency response comprising:

a filter, wherein the filter generates an output signal after removing a frequency from an input signal, the filter comprising a first impedance component and a switch that is connected to the first impedance component, wherein the switch is switched on or off in response to a duty-controlled clock signal; and

a duty ratio controller, wherein the duty ratio controller receives a clock signal and a duty control signal for selectively adjusting the duty-controlled clock signal, controls a duty ratio of the clock signal, and generates the duty-controlled clock signal;

wherein the duty ratio controller comprises: a flip-flop that receives a delayed signal after obtaining the clock signal by a time delay; and a delay component that receives the clock signal, generates the delayed signal, and controls the time delay in response to the duty control signal.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Original) The device of claim 1, wherein the first impedance component and the switch are serially connected between an output node and a voltage node of the filter.

6. (Previously Presented) The device of claim 5, wherein the filter further comprises:

a second impedance component that is connected to an input node and an output node of the filter.

7. (Original) The device of claim 1, wherein the filter further comprises:

an amplifier;

a second impedance component that is connected to one terminal of the amplifier and an output node of the filter; and

a third impedance component that is connected to the one terminal of the amplifier and an input node of the filter, wherein the first impedance component and the switch are serially connected between one terminal of the amplifier and the output node of the filter.

8. (Original) The device of claim 7, wherein the first impedance component is a capacitor, and the second and third impedance components are resistors.

9. (Original) The device of claim 7, wherein the first and third impedance components are resistors, and the second impedance component is a capacitor.

10. (Original) The device of claim 1, wherein the duty ratio of the duty-controlled clock signal is controlled in response to the duty control signal.

11. (Original) The device of claim 1, wherein the switch is a MOS transistor.

12. (Original) The device of claim 1, wherein the switch is positioned in a transmission path.

13. (Original) The device of claim 1, wherein the switch is positioned on a transmission path between an input node and an output node of the device when another transmission path exists between an input node and an output node of the device.

14. (Original) The device of clam 1, wherein the output signal is generated after removing the frequency at a predetermined band from the input signal.

15. (Currently Amended) A device for controlling a frequency response comprising:

a filter, wherein the filter generates an output signal after removing a frequency from an input signal, the filter comprising: an impedance component and a switch that is connected to the impedance component, wherein the switch is switched on or off by a duty-controlled clock signal; and

a duty ratio controller, wherein the duty ratio controller receives a clock signal and a duty control signal for selectively adjusting the duty-controlled clock signal and generates the duty-controlled clock signal,

wherein a frequency response of the filter varies in response to a duty ratio of the duty-controlled clock signal,

wherein the duty ratio controller comprises: a flip-flop that receives a delayed signal after obtaining the clock signal by a time delay; and a delay component that receives the clock signal, generates the delayed signal, and controls the time delay in response to the duty control signal.

16. (Canceled)

17. (Previously Presented) The device of claim 15, wherein the duty ratio controller generates the duty-controlled clock signal in response to the duty control signal.

18. (Original) The device of claim 15, wherein the switch is positioned on a transmission path.

19. (Original) The device of claim 15, wherein the switch is positioned on a transmission path between an input node and an output node of the device when another transmission path exists between an input node and an output node of the device.

20. (Original) The device of claim 15, wherein the output signal is generated after removing the frequency at a predetermined band from the input signal.

21. (New) The device of claim 1, wherein the delay component comprises:

a first inverter that receives the clock signal and the duty control signal and outputs a first inverted clock signal; and

a second inverter that receives the first inverted clock signal the duty control signal and outputs a second inverted clock signal as the delayed signal in response to the duty control signal.